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Debugging Active Optical Devices 1G



Overview

Debugging Active Optical Devices 1G Effective debugging of 1G optical devices involves verifying PHY IP instantiation, SerDes configuration, signal integri.

Key Takeaways

Effective debugging of 1G optical devices involves verifying PHY IP instantiation, SerDes configuration, signal integrity, and link status detection.Key Steps for Debugging

1. Verify PHY IP Core Configuration Ensure that the 1G Ethernet PHY IP (e.g., 1000BASE-X PCS/PMA) is correctly instantiated in your FPGA or SoC design. Check that the QSF settings, dynamic reconfiguration profiles, and clock/reset sequences are properly configured, as misconfiguration can prevent link establishment . Use simulation tools to confirm that TX and RX differential pairs (TXP/TXN, RXP/RXN) are active and correctly mapped . 2. Check Link Status Signals Most PHYs, such as the 88E1512, detect a valid optical signal to assert the link_status register via MDIO. If the link does not come up, verify that the optical module is receiving sufficient optical power and that the signal polarity and encoding match the PHY IP expectations . Ensure that the SFP module is compatible with your IP core and supports 1G operation . 3. Inspect SerDes Configuration 1G SerDes macros often require careful configuration through a shadow register mechanism. Read all shadow registers, modify the necessary bits, and write back to the SerDes macro registers. Incorrect SerDes settings can prevent proper signal alignment and link detection . Use the configuration bus (MCB) to access and verify the 1G SerDes registers. 4. Physical Layer and Optical Checks

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• Confirm that the optical fiber is clean and properly seated.

• Verify that the SFP module is compliant with standards (IEC 60825-1, Class B) and that ESD precautions are followed during handling .

• Check for proper power supply and thermal conditions, as some modules may fail to link under marginal conditions . 5. Use Diagnostic Tools

• MDIO reads can confirm PHY status and error counters.

• Loopback tests at the PHY or MAC level can isolate whether the issue is in the optical link or the IP core.

• Oscilloscope or logic analyzer measurements on TX/RX pairs can help detect signal integrity issues.
Summary

To debug 1G optical devices effectively:

• Confirm PHY IP instantiation and configuration.

• Verify link detection signals and optical power.

• Check SerDes macro settings and shadow registers.

• Inspect physical fiber connections and SFP compliance.

• Use MDIO, loopback, and signal analysis tools to isolate issues. Following these steps ensures that both the FPGA/SoC IP core and the optical module are correctly configured and communicating, minimizing downtime and link failures.

Article Content

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This guide focuses on troubleshooting issues in these two types of systems: the first involves analyzing problems that occur when

7. Troubleshooting and Debugging Diagnostics

The 1G/2.5G/5G/10G Multirate Ethernet PHY IP supports various debugging features, including: This section

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The device logs show alarms such as “Tx Power Low” or “Laser Fault.” DDM parameters indicate the Tx Power is significantly below

Layer 1 Debug Guide

When debugging, always go inward approach for analyzing the PHY command output. In this section, we will discuss, the possible

Ethernet PHY Fiber Debug Guide

For each device, there are fives pins used for fiber communication. However, as best practice, make sure that the PHY is

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When a standards-compliant Powered Device (PD) is connected to a PoE-enabled Ethernet port, it is recognized by a specific

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Debug Tools

There are many tools available to address 1G/10G/25G Ethernet Subsystem design issues. It is important to know which tools are

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7. Troubleshooting and Debugging Diagnostics

This section describes debug methods that support debugging your design in both simulation and hardware

FPGA Debug Fundamentals

The Design Phase Not only is the design captured in this phase, but debugging begins with the use of

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